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[PDF] The Precomputed Branch Architecture

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type requiring a predicted target **address** for the **Precomputed-Branch** architecture is an indirect **jump**, where. the destination may be specified by values ...

www-cse.ucsd.edu/~calder/papers/JSA-99.pdf - [Similar pages](#)

Jan 94 Tips

The programmer replaces the **jump** destination **address** (the trailing 32 bits of 0) at

... By use of constants you can help to compile **precomputed** values. ...

www.mactech.com/articles/mactech/Vol.10/10.01/Jan94Tips/index.html - 56k -

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[PDF] CODE GENERATION FOR EMBEDDED PROCESSORS

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JUMPADR is the. symbolic **jump address**. For every component of the path the

values of the. input ports are **precomputed**. 5.2 Retargetable Code Generation ...

ls12-www.cs.uni-dortmund.de/publications/papers/1995-restart.pdf - [Similar pages](#)

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Precomputed D-Mapping. Assumes all primitives tessellated to same level ... 4-D

address register a0 wo 1; 16 vertex inputs v# ro 1; 16 temporary registers ...

www.microsoft.com/mscorp/corpevents/meltdown2001/ppt/DXG9.ppt - [Similar pages](#)

Microprogramming Details

Mem will take the data in memory at a **precomputed address** (more on this ... **Jump**

- Goto the label specified in the constant column of your microinstruction. ...

www.student.cs.uwaterloo.ca/~cs251/general/microprog.html - 8k -

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[PDF] D1.3 "First-Tier Encryption Definition"

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Control instructions - **jump**, subroutine call, etc. ... |**Jump** to iadr if ZERO flag not set

... as **address** into memory which stores **precomputed** prefixes ...

www.ist-lobster.org/deliverables/d1.3-2.pdf - [Similar pages](#)

Citations: accurate instruction fetch and branch prediction ...

The prediction state comprises target, **address**, and type information as well ... We originally proposed the use of a **Precomputed Branch** architecture in [5]. ...

citeseer.ist.psu.edu/context/109013/0 - 36k - [Cached](#) - [Similar pages](#)

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TBD: Figure out where to **jump** to and put **address** in A1 ... we have sped up our code by storing a table of **precomputed** values at compile time rather than ...

cse.stanford.edu/class/cs110/handouts/17SwitchAndSubs.pdf - [Similar pages](#)

James, Doug

Mailing address: Carnegie Mellon University Robotics Institute 5000 Forbes Avenue Pittsburgh, PA 15213. For more information, see my personal homepage. [Jump ...](#)
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[PPT] 370 lecture

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BTB; Return Address Stack; Precomputed Branch. Recovery logic ... Exceptions are usually handled by jumping into a service (software) routine. ...
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[PPT] Lecture 3: R4000 + Intro to ILP

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condition becomes known late in pipeline. x. A = B op C. Predicated Execution.

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www.cs.berkeley.edu/~kubitron/courses/cs252-F98/lectures/Lec09-prediction.ppt -

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CS252/Kubiatowicz. Lec 11.16. 10/06/00. Dynamic Branch Prediction Summary ...

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Conditional branches in the instruction stream degrade performance. by causing

pipeline flushes. **Branch prediction**. mechanisms can overcome this limitation ...

www.cecs.uci.edu/conference_proceedings/iccd_sudeep.pdf - [Similar pages](#)

interrupts: external events that cause the processor to stop ...

For example, instructions fetched as a result of a **branch prediction**.

advantages/disadvantages of **condition codes** **branch prediction**: rather than wait for

...

www.ece.utexas.edu/~patt/05f.360N/handouts/exam2_annotated_buzzwords.txt - 18k -

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System and method for improving **branch prediction** in compiled ...

A method for optimizing **conditional branch prediction** in a computer program ... The

system 30 includes one or more processors 32, memory 34, and an I/O ...

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POWER4 System Microarchitecture

We designed the entire system, from the processor, to memory and I/O bridge chips, ...

Branch Prediction: To help mitigate the effects of the long pipeline ...

www-1.ibm.com/servers/eserver/pseries/hardware/whitepapers/power4.html - 38k -

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[PS] Improving Static Branch Prediction in a Compiler Brian L. Deitrich ...

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This was done to determine if there are any subroutine types that allow a **branch**

prediction to be made on a **conditional branch** that guards the subroutine's ...

www.crhc.uiuc.edu/IMPACT/ftp/conference/pact-98-branchpred.ps - [Similar pages](#)

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to reduce I/O wait time. A production ODB run typically. uses hundreds of warehouses

and ... prediction experiments. 6.1 Conditional Branch Prediction ...
www.iccd-conference.org/proceedings/2002/17000242.pdf - Similar pages

[PS] A Study of Dynamic Branch Prediction for SHARC DSPs Suleyman Sair ...

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Branch prediction has been a popular architectural feature used to remedy the negative effects of **conditional** control transfer. We believe that dynamic ...
www.ece.neu.edu/info/architecture/publications/cases.ps.gz - Similar pages

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Such hardware allows for improvements of **branch prediction** accuracy, but **branch** ...
 It also often leads to the elimination of **conditional branch** ...
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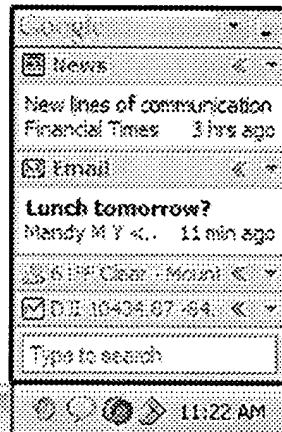
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